EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5	((design adj rules adj checker) or CRS) and (noise adj3 analysis) and PCB	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 16:28
L2	1	((design adj rules adj checker) or DRC) and (noise adj3 analysis) and PCB	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 16:26
L3	0	(design adj rules adj checker) and (noise adj3 analysis) and PCB	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 16:27
L4	9	(noise adj3 analysis) same PCB	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 16:27
L5	0	(design adj rules adj checker) and (noise adj3 analysis) and PCB	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 16:29
L6	0	(design adj rules adj checker) and (noise with analysis) and PCB	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 16:29
L7	0	(design adj rules adj checker) and noise and PCB	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 16:29
L8	26	DRC and noise and PCB	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 16:30

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L9	31	("4115003" \| "4768154" \| "4991115" \| "5019970" \| "5028866" \| "5062054" \| "5109479" \| "5160842" \| "5297053" \| "5299268" \| "5392222" \| "5440651").PN. OR ("5781446").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/19 16:32
L10	2	("5781446" \| "6185722").PN. OR ("6865724").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/19 16:44

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  ```

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  ```
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  ```

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  John Colter, Netscape Navigator
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  "museum of natural history" "museum of modern art"
  ```

- Narrow your searches by using a + if a search term must appear on a page.

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  museum +art
  ```

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```

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1 Crosstalk noise analysis: A simplified transmission-line based crosstalk noise model for on-chip RLC wiring

Kanak Agarwal, Dennis Sylvester, David Blaauw

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press , IEEE Press

Full text available: pdf(232.14 KB) Publisher Site

Additional Information: full citation, abstract, references

In this paper, we present a new RLC crosstalk noise model that combines simplicity, accuracy, and generality. The new model is based on transmission line theory and is applicable to asymmetric driver and line configurations. The results show that the model captures both the waveform shape and peak noise accurately (average error in peak noise was 6.5%). A key feature of the new model is that its derivation and form enables physical insight into the dependency of total coupling noise on relevant ...

2 Time synch and localization: Asymptotically optimal time synchronization in dense sensor networks

An-swol Hu, Sergio D. Servetto

September 2003 **Proceedings of the 2nd ACM international conference on Wireless sensor networks and applications**

Publisher: ACM Press

Full text available: pdf(195.22 KB)

Additional Information: full citation, abstract, references, citings, index terms

We consider the problem of synchronization of all clocks in a sensor network, in the regime of asymptotically high node densities. We formulate this problem as one in which all clocks must line up with the clock of an arbitrary node in the network (of course *without* assuming that this clock can be observed everywhere in the network, nor assuming that this node has any special hardware--this node could be any). We give a state-space description for the generation of observable data as a fu ...

3 Optimal sizing of high-speed clock networks based on distributed RC and lossy transmission line models

Qing Zhu, Wayne W.-M. Dai, Joe G. Xi

November 1993 **Proceedings of the 1993 IEEE/ACM international conference on**

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1 Electromagnetic modeling and signal integrity simulation of power/ground networks in high speed digital packages and printed circuit boards

Frank Y. Yuan

May 1998 **Proceedings of the 35th annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(275.46 KB) Publisher Site

Additional Information: full citation, abstract, references, index terms

The electromagnetic modeling and parameter extraction of digital packages and PCB boards for system signal integrity applications are presented. A systematic approach to analyze complex power/ground structures and simulate their effects on digital systems is developed. First, an integral equation boundary element algorithm is applied to the electromagnetic modeling of the PCB structures. Then, equivalent circuits of the power/ground networks are extracted from the EM solution. In an integra ...

Keywords: custom sizing, migration, timing optimazation

2 System simulation of printed circuit boards including packages and connectors

K. Adamiak, R. Allen, J. Poltz, C. Rebizant, A. Wexler

January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Publisher: ACM Press

Full text available: pdf(573.59 KB)

Additional Information: full citation, abstract, references, citings, index terms

An efficient method for analog simulation of printed circuit board systems is proposed. It is based on the transmission line model derived from the analysis of the electromagnetic field in a two-dimensional cross-section of devices. Simulation results for two circuits with IC package, cable and connector models are presented. The results confirm the effectiveness of this method.

3 Effects of correlations on accuracy of power analysis—an experimental study

P. Schneider, S. Krishnamoorthy

August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design**

Publisher: IEEE Press

Full text available: pdf(106.45 KB) Additional Information: full citation, references, citings, index terms

4 EMC-driven midway routing on PCBs

H. Schmidt, D. Theune, R. Thiele, T. Lengauer

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(731.89 KB) Publisher Site Additional Information: full citation, abstract

Phenomena of electromagnetic compatibility (EMC) have to be considered during layout synthesis of printed-circuit boards (PCBs), in order to design failsafe and high-performance systems. In this paper the PCB routing-system HERO, presented in a previous publication, is extended by a new layer-assignment/net-ordering phase, called midway routing, performed after global and before detailed routing. The new method yields a significantly increased completion rate, improved EMC-behavior, and fewer la ...

Keywords: EMC-driven midway routing, HERO, PCB layout, PCB routing-system, circuit layout CAD, electromagnetic compatibility, layer-assignment, layout synthesis, midway routing, net-ordering phase, network routing, network topology, printed circuit layout, printed-circuit boards

5 HERO: hierarchical EMC-constrained routing

D. Theune, R. Thiele, T. Lengauer, A. Feldmann

November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

Full text available: pdf(726.00 KB) Additional Information: full citation, references, citings, index terms

6 Prediction of radiated electromagnetic emissions from PCB traces based on green dyadics

E. Leroux, F. Canavero, G. Vecchi

December 1995 **Proceedings of the conference on European design automation**

Publisher: IEEE Computer Society Press

Full text available: pdf(583.74 KB) Additional Information: full citation, references, index terms

7 Performance driven global routing and wiring rule generation for high speed PCBs and MCMs

Sharad Mehrotra, Paul Franzon, Michael Steer

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Publisher: ACM Press

Full text available: pdf(218.71 KB) Additional Information: full citation, references, citings, index terms

8 An efficient methodology for extraction and simulation of transmission lines for application specific electronic modules

S. Y. Kim, E. Tuncer, R. Gupta, B. Krauter, T. Savarino, D. P. Neikirk, L. T. Pillage

November 1993 **Proceedings of the 1993 IEEE/ACM international conference on**

Computer-aided design
Publisher: IEEE Computer Society Press
Full text available: pdf(820.96 KB) Additional Information: full citation, references, citings

9 Design support of printed circuit boards concerning radiation and irradiation effects (EMI): using an extended EMC-Workbench
Stefan Öing, Werner John
September 1994 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(491.86 KB) Additional Information: full citation, references, index terms

10 Bounds on net lengths for high-speed PCB
Jaebum Lee, Eugene Shragowitz, David Poli
November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society Press
Full text available: pdf(378.06 KB) Additional Information: full citation, references, citings

11 IPDA: interconnect performance design assistant
N. H. Chang, K.-J. Chang, J. Leo, K. Lee, S.-Y. Oh
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(617.13 KB) Additional Information: full citation, references, index terms

12 Knowledge based approach for the verification of CAD database generated by an automated schematic capture system
J. Y. Tou, W. H. Ki, K. C. Fan, C. L. Huang
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(765.41 KB) Additional Information: full citation, abstract, references, index terms

CAD database generated by an automatic schematic capture system needs to be verified before it can be used in design automation. This verification is best performed by a knowledge-based expert system. Presented in this paper is the design of a knowledge-based system for the verification of CAD database generated by AUTORED. Database-driven, pattern-directed inference technique is employed to identify and correct erroneous data records due to misrecognition. This knowledge-based verification ...

13 Comparison of connection admission-control schemes in the presence of hand-offs in cellular networks
Sunghyun Choi, Kang G. Shin
October 1998 **Proceedings of the 4th annual ACM/IEEE international conference on Mobile computing and networking**
Publisher: ACM Press
Full text available: pdf(1.98 MB) Additional Information: full citation, references, citings, index terms

14 Fast simulation method for the detection of reflection—and crosstalk effects during the design of complex printed circuit boards
E. Griese, J. Schrage, M. Vogt
September 1994 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(544.92 KB) Additional Information: full citation, references, index terms

15 Abstract routing of logic networks for custom module generation
S. T. Healey, W. J. Kubitz
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(845.98 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a switchbox-type router for custom VLSI module generation as performed by a module planner. A module is decomposed into abstract cells consisting of global routes and Boolean functional specifications. Each abstract cell is given to a cell synthesizer which generates the circuit layout and through-the-cell routing. Abstract routing for a module planner is in some sense similar to switchbox routing to the degree that all of the routes are generated inter ...

16 Experience in designing a large-scale multiprocessor using field-programmable devices and advanced CAD tools
S. Brown, N. Manjikian, Z. Vranesic, S. Caranci, A. Grbic, R. Grindley, M. Gusat, K. Loveles, Z. Zilic, S. Srbljic
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(104.47 KB) Additional Information: full citation, references, citings, index terms

17 Rapid prototyping of ASIC based systems
P. H. Kelly, K. J. Page, P. M. Chau
June 1994 **Proceedings of the 31st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(139.19 KB) Additional Information: full citation, references, index terms

18 Basic concepts of timing-oriented design automation for high-performance mainframe computers
Hidekazu Terai, Fumio Goto, Katsuro Wakai, Tokinori Kozawa, Mitsugu Edagawa, Satoshi Hososaka, Masahiro Hashimoto
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**
Publisher: ACM Press
Full text available: pdf(716.84 KB) Additional Information: full citation, references, citings, index terms

19 Synthesis of BIST hardware for performance testing of MCM interconnections
Rajesh Pendurkar, Abhijit Chatterjee, Yervant Zorian
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on**

Computer-aided design
Publisher: ACM Press
Full text available: pdf(507.34 KB) Additional Information: full citation, references, citings, index terms

20 Assessing the cost effectiveness of integrated passives
Michael Scheffler, Gerhard Tröster
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: ACM Press
Full text available: pdf(115.70 KB) Publisher Site Additional Information: full citation, references, index terms

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L1	1	("5596506").PN.	USPAT	OR	OFF	2006/05/19 10:53
L2	908	((circuit adj board) or PCB) and topology and waveform and noise	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 10:54
L3	176	2 and (circuit with analysis)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 10:55
L4	18	3 and (noise with analysis)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 10:56
L5	16	("3370294" \| "3462561" \| "3465106" \| "3723883" \| "4493092" \| "4507793" \| "4645883" \| "4686703" \| "4727543" \| "4998079" \| "5175515").PN. OR ("5757654"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/19 12:03
L6	8	("5502644" \| "5546321" \| "5610833" \| "5708587" \| "5757654" \| "6058256" \| "6161215" \| "6484299").PN. OR ("6567955"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/19 12:43
L7	53	(circuit adj3 analysis) and (judgement with result)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 12:43
L8	9	(circuit adj3 analysis) and (judgement adj3 result)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 12:43

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("5596506").PN.	USPAT	OR	OFF	2006/05/19 10:53
L2	908	((circuit adj board) or PCB) and topology and waveform and noise	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 10:54
L3	176	2 and (circuit with analysis)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 10:55
L4	18	3 and (noise with analysis)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/19 10:56
L5	16	("3370294" \| "3462561" \| "3465106" \| "3723883" \| "4493092" \| "4507793" \| "4645883" \| "4686703" \| "4727543" \| "4998079" \| "5175515").PN. OR ("5757654").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/19 12:03
L6	8	("5502644" \| "5546321" \| "5610833" \| "5708587" \| "5757654" \| "6058256" \| "6161215" \| "6484299").PN. OR ("6567955").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/19 12:36